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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,549	KNEBEL ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/06/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities: in the 1st line of claim 1, "I method" is incorrect. It should be --A method--. Appropriate correction is required.

2. Claim 14 is objected to because of the following informalities: in the 2-3 lines of claim 14, "step performing" is incorrect. It should be –step of performing--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1, 2, 3, 4, 5, 6, 7, 8, 13, 20, 21, 23, 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kirkpatrick et al. (US 2002/0167282 A1) in view of Jania et al. (US 3,575,256).

As per claim 1, Kirkpatrick et al. teach a method of frequency modification for one or more electronic components in an electronic system, the method comprising the steps of: the one or more performance parameters correlated with maximum operating frequency of one or more electronic components of the electronic system; and adjusting an operating frequency of the one or more electronic components from the electronic system in accordance with the one or more performance parameters (page 7, paragraph 122, page 39, paragraph 761, 764, Kirkpatrick et al.).

However Kirkpatrick et al. do not explicitly teach the specific use of determining, at a particular age of the electronic system, one or more performance parameters for the electronic system.

Jania et al. in an analogous art teach system performance of changes in the device parameters with temperature, age and supply voltage (col. 25, lines 73-75, Jania et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kirkpatrick et al.'s patent with the teachings of Jania et al. by including an additional step of determining, at a particular age of the electronic system, one or more performance parameters for the electronic system.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that determining, at a particular age of the electronic system, one or more performance parameters for the electronic system would provide the opportunity to modify the aged system to operate the system at peak performance.

- As per claim 2, Kirkpatrick et al. and Jania et al. teach the additional limitations.

Kirkpatrick et al. teach the method, wherein the step of adjusting adjusts the operating frequency to an adjusted operating frequency, and wherein the adjusted operating frequency is less than or equal to the maximum operating frequency of the one or more electronic components for the particular age of the system (page 7, paragraph 122, Kirkpatrick et al.).

- As per claim 3, Kirkpatrick et al. and Jania et al. teach the additional limitations.

Kirkpatrick et al. teach the method, wherein a given one of the one or more performance parameters can be converted to a selected operating frequency to be used in the step of adjusting (page 7, paragraph 122, Kirkpatrick et al.).

- As per claim 4, Kirkpatrick et al. and Jania et al. teach the additional limitations.

Kirkpatrick et al. teach the method, wherein the given performance parameter comprises a multiplicand used to convert a base frequency to the selected operating frequency to be used in the step of adjusting (page 7, paragraph 122, page 45, paragraph 857, Kirkpatrick et al.).

- As per claim 5, Kirkpatrick et al. and Jania et al. teach the additional limitations.

Jania et al. teach the step of determining a performance parameter further comprises the steps of determining whether the particular age of the electronic system is a predetermined age (col. 25, lines 73-75, Jania et al.). Kirkpatrick et al. teach determining an operating frequency from the one or more performance parameters when the particular age is the given age (page 39, paragraph 764, Kirkpatrick et al.).

- As per claim 6, Kirkpatrick et al. and Jania et al. teach the additional limitations.

Kirkpatrick et al. teach the method, wherein a given one of the one or more performance parameters comprises a predetermined operating frequency to be used in the steps of determining and adjusting (page 7, paragraph 122, page 39, paragraph 764, Kirkpatrick et al.).

- As per claim 7, Kirkpatrick et al. and Jania et al. teach the additional limitations.

Jania et al. teach the method, wherein the step of determining, at a particular age of the electronic system, a performance parameter for the electronic system (col. 25, lines 73-75, Jania et al.). Kirkpatrick et al. teach the step of gathering, at the particular age of the electronic system, performance statistics from one or more feedback circuits, and determining whether actual performance of the electronic system should be adjusted by using the performance statistics (fig. 343, pages 62-63, paragraph 1098, Kirkpatrick et al.).

- As per claim 8, Kirkpatrick et al. and Jania et al. teach the additional limitations.

Kirkpatrick et al. teach the method, wherein the step of gathering, at the particular age of the electronic system, performance statistics from one or more feedback circuits, further comprises the step of gathering, at the particular age of the electronic system, performance statistics (fig. 343, pages 62-63, paragraph 1098, Kirkpatrick et al.).

Jania et al. teach one or more age monitoring circuits (col. 25, lines 73-75, Jania et al.).

- As per claim 13, Kirkpatrick et al. and Jania et al. teach the additional limitations.

Kirkpatrick et al. teach the method wherein the one or more performance parameters comprise one or more of previous operating frequency (page 7, paragraph 122, page 39, paragraph 764, Kirkpatrick et al.).

Jania et al. teach that one or more performance parameters comprise ambient temperature, hours of operation, and supply voltage (col. 25, lines 73-75, Jania et al.).

- As per claim 20, Kirkpatrick et al. and Jania et al. teach the additional limitations.

Kirkpatrick et al. teach an electronic system able to perform frequency modification for electronic components, the electronic system comprising: one or more electronic components; at least one clock generation circuit coupled to the one or more electronic components and adapted to: the one or more performance parameters correlated with maximum operating frequency of one or more electronic components of the electronic system; and adjust an operating frequency of the one or more electronic components from the electronic system in accordance with the one or more performance parameters (fig. 342, page 7, paragraph 122, page 39, paragraph 761, 764, page 62, paragraph 1088, Kirkpatrick et al.).
Jania et al. teach to determine, at a particular age of the electronic system, one or more performance parameters for the electronic system (col. 25, lines 73-75, Jania et al.).

- As per claim 21, Kirkpatrick et al. and Jania et al. teach the additional limitations.

Kirkpatrick et al. teach the electronic system, wherein the performance parameters comprise: a corresponding plurality of predetermined operating frequencies; the at least one clock generation circuit comprises a wear-out clock; and the wear-out clock is further adapted to adjust operating frequency of the one or more electronic components by adjusting a current operating frequency of the one or more electronic components to a predetermined operating frequency corresponding to the given predetermined age (fig. 342, page 7, paragraph 122, page 39, paragraph 764, page 62, paragraph 1088, Kirkpatrick et al.).
Jania et al. teach that the performance parameters comprise a plurality of predetermined ages and at a particular age of the electronic system, one or more of the predetermined ages and to determine whether a current age of the electronic system corresponds to a given one of the predetermined ages (col. 25, lines 73-75, Jania et al.).

- As per claim 23, Kirkpatrick et al. and Jania et al. teach the additional limitations.

Kirkpatrick et al. teach the electronic system, wherein the at least one clock generation circuit further comprises a performance control unit (fig. 342, 343, page 62, paragraph 1088, pages 62-63, paragraph 1098, Kirkpatrick et al.).

- As per claim 24, Kirkpatrick et al. and Jania et al. teach the additional limitations.

Kirkpatrick et al. teach the electronic system, further comprising one or more feedback circuits in the one or more electronic components, the one or more feedback circuits coupled to the performance control unit (fig. 342, 343, page 62, paragraph 1088, 1089, pages 62-63, paragraph 1098, Kirkpatrick et al.).

6. Claims 9, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kirkpatrick et al. (US 2002/0167282 A1) and Jania et al. (US 3,575,256) as applied to claim 8 above, and further in view of Wu et al. (Bipolar Bootstrapped Multi-emitter BiCMOS (B^2M-BiCMOS) Logic for Low-Voltage Applications, Electronics, Circuits, and Systems, 1996, Volume 2, Pages: 1174-1177).

As per claim 9, Kirkpatrick et al. and Jania et al. substantially teach the claimed invention described in claim 8 (as rejected above).

However Kirkpatrick et al. and Jania et al. do not explicitly teach the specific use of the step of determining, at the particular age of the electronic system, a given performance statistic by comparing speed of an aged circuit with speed of a test circuit that is enabled only for the comparison, wherein the aged circuit has been operated for approximately the particular age.

Wu et al. in an analogous art teach to compare speed performance of the new BiCMOS logic circuit with those of CMOS, conventional BiCMOS, and Bootstrapped BiCMOS (BS-BiCMOS) logic circuits (abstract, Wu et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kirkpatrick et al.'s patent with the teachings of Wu et al. by including an additional step of determining, at the particular age of the electronic system, a given performance statistic by comparing speed of an aged circuit with speed of a test circuit that is enabled only for the comparison, wherein the aged circuit has been operated for approximately the particular age.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to determine if the aged circuit is performing at the same speed as the new circuit.

- As per claim 25, Kirkpatrick et al., Jania et al. and Wu et al. teach the additional limitations.

Kirkpatrick et al. teach the electronic system, wherein a given one of the one or more performance parameters comprises one or more performance statistics (page 39, paragraph 764, Kirkpatrick et al.) and a given one of the feedback circuits comprises an age-monitoring circuit (fig. 342, page 62, paragraph 1088, Kirkpatrick et al.).

Wu et al. teach an aged circuit and a new circuit, wherein the performance control unit is adapted to enable the new circuit only during a comparison between the aged and new circuits and to determine the one or more performance statistics from the comparison, wherein the aged circuit has been operated for approximately the particular age (abstract, Wu et al.).

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kirkpatrick et al. (US 2002/0167282 A1) and Jania et al. (US 3,575,256) as applied to claim 7 above, and further in view of Chur (US 5,124,849).

As per claim 10, Kirkpatrick et al. and Jania et al. substantially teach the claimed invention described in claim 7 (as rejected above).

However Kirkpatrick et al. and Jania et al. do not explicitly teach the specific use of the step of gathering, at the particular age of the electronic system, performance statistics from one or more error detecting circuits.

Chur in an analogous art teaches testing of completed head disk assemblies (HDA)...develop into a problem as the HDA ages (col. 15, lines 57-68, Chur).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kirkpatrick et al.'s patent with the teachings of Chur by including an additional step of gathering, at the particular age of the electronic system, performance statistics from one or more error detecting circuits.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that gathering, at the particular age of the electronic system, performance statistics from one or more error detecting circuits would provide the opportunity to determine the number of errors in the aged circuit operation.

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kirkpatrick et al. (US 2002/0167282 A1), Jania et al. (US 3,575,256) and Chur (US 5,124,849) as applied to claim 10 above, and further in view of Ohie et al. (US 5,936,448).

As per claim 11, Kirkpatrick et al., Jania et al. and Chur substantially teach the claimed invention described in claim 10 (as rejected above). Chur also teaches the step of determining that one or more errors have occurred (col. 15, lines 57-68, Chur).

However Kirkpatrick et al., Jania et al. and Chur do not explicitly teach the specific use of the steps of lowering operating frequency from a current operating frequency, beginning execution at a point before the one or more errors occurred, determining if the one or more errors reoccur, and if the one or more errors do not reoccur, leaving the lowered operating frequency as the current operating frequency.

Ohie et al. in an analogous art teach that to reduce these measuring errors, the noise supply is decreased by lowering the operating frequency while threshold voltages are measured (col. 1, lines 55-57, Ohie et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kirkpatrick et al.'s patent with the teachings of Ohie et al. by including an additional step of lowering operating frequency from a current operating frequency, beginning execution at a point before the one or more errors occurred, determining if the one or more errors reoccur, and if the one or more errors do not reoccur, leaving the lowered operating frequency as the current operating frequency.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to reduce the occurrence of errors by lowering the operating frequency.

9. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kirkpatrick et al. (US 2002/0167282 A1), Jania et al. (US 3,575,256), Chur (US 5,124,849) and Ohie et al. (US 5,936,448) as applied to claim 11 above, and further in view of Burns et al. (US 4,698,587).

As per claim 12, Kirkpatrick et al., Jania et al., Chur and Ohie et al. substantially teach the claimed invention described in claim 11 (as rejected above).

However Kirkpatrick et al., Jania et al., Chur and Ohie et al. do not explicitly teach the specific use of before the step of lowering operating frequency, the steps of beginning execution at a point before the one or more errors occurred, determining if the one or more errors reoccur, and if the one or more errors do not reoccur, leaving current operating frequency alone.

Burns et al. in an analogous art teach determining the maximum operating frequency for which the integrated circuit operates correctly (no logic errors), (col. 8, lines 17-20, Burns et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kirkpatrick et al.'s patent with the teachings of Burns et al. by including additionally before the step of lowering operating frequency, the steps of beginning execution at a point before the one or more errors occurred, determining if the one or more errors reoccur, and if the one or more errors do not reoccur, leaving current operating frequency alone.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to determine the maximum operating frequency in an electronic system where no errors occur.

10. Claims 14, 15, 16, 17, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kirkpatrick et al. (US 2002/0167282 A1) and Jania et al. (US 3,575,256) as applied to claim 1 above, and further in view of Bassett et al. (US 5,127,008).

As per claim 14, Kirkpatrick et al. and Jania et al. substantially teach the claimed invention described in claim 1 (as rejected above). Kirkpatrick et al. also teach the method, wherein the one or more performance parameters are stored performance parameters (page 39, paragraph 764, Kirkpatrick et al.).

However Kirkpatrick et al. and Jania et al. do not explicitly teach the specific use of performing reliability testing to determine wear-out information.

Basett et al. in an analogous art teach that the second module testing process is performed when it is necessary to enhance the operational reliability of shipped modules, by accelerating and provoking the immediate failure of those correctly but marginally fabricated devices and modules which would otherwise fail early in their expected operational lifespan (col. 1, lines 52-57, Basett et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kirkpatrick et al.'s patent with the teachings of Basett et al. by including an additional step of performing reliability testing to determine wear-out information.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that performing reliability testing to determine wear-out information would provide the opportunity to determine the reliability of electronic components.

- As per claim 15, Kirkpatrick et al., Jania et al. and Bassett et al. teach the additional limitations.

Jania et al. teach the method, wherein the stored performance parameters comprise predetermined ages (col. 25, lines 73-75, Jania et al.).

Kirkpatrick et al. teach predetermined operating frequencies at corresponding ones of the predetermined ages (page 39, paragraph 764, Kirkpatrick et al.).

- As per claim 16, Kirkpatrick et al., Jania et al. and Bassett et al. teach the additional limitations.

Kirkpatrick et al. teach the step of determining one or more prior operating frequencies of the electronic system (page 7, paragraph 122, page 39, paragraph 764, Kirkpatrick et al.).

Jania et al. teach one or more ambient temperatures surrounding the electronic system, and one or more supply voltages of the electronic system (col. 25, lines 73-75, Jania et al.).

- As per claim 17, Kirkpatrick et al., Jania et al. and Bassett et al. teach the additional limitations.

Bassett et al. teach the method, further comprising the step of providing supply voltage for the electronic system that is higher than nominal supply voltage (col. 1, lines 58-62, Bassett et al.).

- As per claim 18, Kirkpatrick et al., Jania et al. and Bassett et al. teach the additional limitations.

Bassett et al. teach the method, further comprising the step of providing ambient temperature surrounding the electronic system that is higher than nominal ambient temperature (col. 1, lines 58-62, Bassett et al.).

11. Claims 19, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kirkpatrick et al. (US 2002/0167282 A1) and Jania et al. (US 3,575,256) as applied to claim 1 above, and further in view of Kolanek (US 2002/0047745 A1).

As per claim 19, Kirkpatrick et al. and Jania et al. substantially teach the claimed invention described in claim 1 (as rejected above).

However Kirkpatrick et al. and Jania et al. do not explicitly teach the specific use of the method, wherein the performance parameters are received from an external source.

Kolanek in an analogous art teaches that the set of desired or set point values for the performance parameters, which are provided to the SLMC 320 from some external source such as a wireless communication network system operator (page 5, paragraph 60, Kolanek).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kirkpatrick et al.'s patent with the teachings of Kolanek by including an additional step of using the method, wherein the performance parameters are received from an external source.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the method, wherein the performance parameters are received from an external source would provide the opportunity to control the performance of the system externally.

- As per claim 22, Kirkpatrick et al., Jania et al. and Kolanek teach the additional limitations.

Kolanek teaches the electronic system, wherein the wear-out clock is further adapted to retrieve the predetermined ages and corresponding predetermined operating frequencies from a source external to the wear-out clock (page 5, paragraph 60, Kolanek).

12. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kirkpatrick et al. (US 2002/0167282 A1) and Jania et al. (US 3,575,256) as applied to claim 24 above, and further in view of Chur (US 5,124,849) and Ohie et al. (US 5,936,448).

As per claim 26, Kirkpatrick et al. and Jania et al. substantially teach the claimed invention described in claim 24 (as rejected above). Kirkpatrick et al. also teach the electronic system, wherein a given one of

the one or more performance parameters comprises one or more performance statistics (page 39, paragraph 764, Kirkpatrick et al.).

However Kirkpatrick et al. and Jania et al. do not explicitly teach the specific use of a given one of the feedback circuits comprises an error detecting circuit, the error detecting circuit adapted to determine if an error occurs, wherein the one or more performance statistics indicate than an error has occurred.

Chur in an analogous art teaches testing of completed head disk assemblies (HDA)...develop into a problem as the HDA ages (col. 15, lines 57-68, Chur).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kirkpatrick et al.'s patent with the teachings of Chur by including an additional step of using a given one of the feedback circuits comprises an error detecting circuit, the error detecting circuit adapted to determine if an error occurs, wherein the one or more performance statistics indicate than an error has occurred.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to determine the number of errors in the aged circuit operation.

Kirkpatrick et al. and Jania et al. also do not explicitly teach specifically that the performance control unit is further adapted to receive the one or more performance statistics, indicating that one or more errors have occurred, from the error detection circuit, to lower operating frequency from a current operating frequency, to cause execution to begin at a point before the one or more errors occurred, to determine if the error reoccurs, and if the error does not reoccur, to leave the lowered operating frequency as the current operating frequency.

However Ohie et al. in an analogous art teach that to reduce these measuring errors, the noise supply is decreased by lowering the operating frequency while threshold voltages are measured (col. 1, lines 55-57, Ohie et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kirkpatrick et al.'s patent with the teachings of Ohie et al. by including additionally that the performance control unit is further adapted to receive the one or more performance statistics, indicating

that one or more errors have occurred, from the error detection circuit, to lower operating frequency from a current operating frequency, to cause execution to begin at a point before the one or more errors occurred, to determine if the error reoccurs, and if the error does not reoccur, to leave the lowered operating frequency as the current operating frequency.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to reduce the occurrence of errors by lowering the operating frequency.

13. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kirkpatrick et al. (US 2002/0167282 A1) and Jania et al. (US 3,575,256) as applied to claim 20 above, and further in view of Iida et al. (US 6,525,585 B1).

As per claim 27, Kirkpatrick et al. and Jania et al. substantially teach the claimed invention described in claim 20 (as rejected above).

However Kirkpatrick et al. and Jania et al. do not explicitly teach the specific use of the electronic system, wherein the at least one clock generation circuit further comprises an oscillator and one or more frequency multipliers, the oscillator having an output, each of the one or more of the frequency multipliers having an input and output, the output of the oscillator coupled to an input of each of the one or more frequency multipliers, a given one of the one or more electronic components coupled to an output of a given one of the one or more frequency multipliers, and wherein the at least one clock generation circuit is further adapted to create an adjusted operating frequency for the given electronic component by adjusting one or more of the following: operating frequency of the oscillator and a multiplicand used in the given frequency multiplier.

Iida et al. in an analogous art teach that the clock generation circuit...manufacture (fig. 6, col. 3, lines 52-61, Iida et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kirkpatrick et al.'s patent with the teachings of Iida et al. by including an additional step of using the electronic system, wherein the at least one clock generation circuit further comprises an oscillator and one or more frequency multipliers, the oscillator having an output, each of the one or more

of the frequency multipliers having an input and output, the output of the oscillator coupled to an input of each of the one or more frequency multipliers, a given one of the one or more electronic components coupled to an output of a given one of the one or more frequency multipliers, and wherein the at least one clock generation circuit is further adapted to create an adjusted operating frequency for the given electronic component by adjusting one or more of the following: operating frequency of the oscillator and a multiplicand used in the given frequency multiplier.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to adjust the operating frequency of the electronic component to meet the performance requirements.

14. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kirkpatrick et al. (US 2002/0167282 A1) in view of Jania et al. (US 3,575,256) and Takahashi (US 6,253,358 B1).

As per claim 28, Kirkpatrick et al. teach an article of manufacture for performing frequency modification for electronic components, the article of manufacture comprising: the one or more performance parameters correlated with maximum operating frequency of one or more electronic components of the electronic system; and adjusting an operating frequency of the one or more electronic components from the electronic system in accordance with the one or more performance parameters (page 7, paragraph 122, page 39, paragraph 761, 764, Kirkpatrick et al.).

However Kirkpatrick et al. do not explicitly teach the specific use of determining, at a particular age of the electronic system, one or more performance parameters for the electronic system.

Jania et al. in an analogous art teach system performance of changes in the device parameters with temperature, age and supply voltage (col. 25, lines 73-75, Jania et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kirkpatrick et al.'s patent with the teachings of Jania et al. by including an additional step of determining, at a particular age of the electronic system, one or more performance parameters for the electronic system.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that determining, at a particular age

of the electronic system, one or more performance parameters for the electronic system would provide the opportunity to modify the aged system to operate the system at peak performance.

Kirkpatrick et al. also do not explicitly teach the specific use of a computer readable medium containing one or more programs which when executed implement the steps.

However Takahashi in an analogous art teaches that a computer-readable medium... perform the steps (col. 18, lines 60-64, Takahashi).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kirkpatrick et al.'s patent with the teachings of Takahashi by including an additional step of using a computer readable medium containing one or more programs which when executed implement the steps.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a computer readable medium containing one or more programs which when executed implement the steps would provide the opportunity to perform the steps fast and accurately.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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